

Amendments

In the Claims:

1. (Currently Amended) A digital control logic circuit having a characteristic of time hysteresis for controlling transition of a digital control signal during a predetermined period, comprising:

a first time hysteresis unit having a characteristic of time hysteresis by latching an input signal for predetermined time of a first delay when an input signal transits from a first level to a second level; and

a second time hysteresis unit connected in series to the first time hysteresis unit having a characteristic of time hysteresis by latching the input signal for predetermined time of a second delay longer than the first delay when the input signal transits from the second level to the first level.

2. (Original) The circuit according to claim 1, further comprising an inverter for inverting an output signal from said second time hysteresis unit.

3. (Currently Amended) The circuit according to claim 1, wherein the first time hysteresis unit comprises:

a latch unit for maintaining an output signal at a predetermined level;
an inverter for inverting the output signal from the latch unit; and
a first delay unit connected to the latch unit in a feedback structure, which delays an output signal from the inverter for predetermined time ~~of a first~~ of the first delay.

4. (Currently Amended) The circuit according to ~~claim 1~~ claim 3, wherein the second time hysteresis unit comprises:

a latch unit maintaining an output signal at a predetermined level;
an inverter for inverting the output signal from the latch unit; and

a second delay unit connected to the latch unit in a feedback structure, which delays an output signal from the inverter for predetermined time ~~of a second~~ of the second delay.

5. (Currently Amended) The circuit according to ~~claim 3~~ claim 1, wherein the second delay time is more than two times longer than the first delay time.

Claims 6 and 7 (Cancelled).

8. (Previously Presented) The circuit according to claim 4, wherein the second delay time is more than two times longer than the first delay time.